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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,599	03/31/2004	Gansha Wu	42339-198432	4361

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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

E

Office Action Summary	Application No.	Applicant(s)	
	10/813,599	WU ET AL.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is no antecedent basis for the term "computer accessible medium."

Claim Objections

1. The term "stack-state-aware translation" is not a term well-known in the art, nor is it defined within the claim to allow one of ordinary skill in the pertinent art to ascertain what the term means. Further, the specification does not supply an ***explicit*** definition to bring into the claims. Correction is not required, but the examiner must now take the broadest reasonable interpretation of the term and the claims as written may prove difficult to enforce as written if a patent should issue.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Lindwer (US Patent 6,298,434).

4. As per claim 1:

A method to execute an instruction on an operand stack, the method comprising:

performing a stack-state-aware translation of the instruction to threaded code to determine an operand stack state for the instruction (column 11, lines 3-22) (the preprocessor moves items from registers to memory and adjusts the SP for the instructions);

dispatching the instruction according to the operand stack state for the instruction (inherent); and

executing the instruction (inherent).

5. As per claim 2:

The method according to claim 1, said performing comprising:

determining a number of operands on the operand stack before the instruction is executed (column 11, lines 3-22) (It is inherent that this step will be taken in moving items from registers to memory and adjusting the SP for the instructions);

determining a number of operands on the operand stack after the instruction is executed based on a number of operands that the instruction consumes and a number of operands that the instruction produces (column 11, lines 3-22); and

inferring a number of shift operations required after execution of the instruction to maintain top-of-stack elements (column 11, lines 3-22).

6. As per claim 3:

The method according to claim 2, wherein the number of shift operations required after execution of the instruction is based on the number of operands on the operand stack before the instruction is executed and the number of operands on the operand stack after the instruction is executed (column 11, lines 15-22).

7. As per claim 4:

The method according to claim 2, wherein the number of shift operations required after execution of the instruction is inferred based on a static lookup table (column 6, lines 39-47) (The translation is based on a static table. Through the table, it is known how many operands will be used and how many will be placed back on the stack, and based on that is how many items are transferred to memory.).

8. As per claim 5:

The method according to claim 1, wherein the operand stack is a mixed-register stack (column 11, lines 15-22).

9. As per claim 6:

The method according to claim 1, wherein the operand stack state comprises a number of shift operations to maintain top-of-stack elements of the operand stack after the execution of the instruction (column 11, lines 15-22).

10. As per claim 7:

The method according to claim 6, wherein the top-of-stack elements comprise a register stack (column 11, lines 15-22).

11. As per claim 8:

The method according to claim 1, further comprising:

refilling the operand stack (column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

12. As per claim 9:

A system comprising:

an operand stack to execute an instruction (column 11, lines 3-5); and

an interpreter to determine a state of the operand stack, translate the instruction into threaded code, and dispatch the instruction based on the state of the operand stack (column 11, lines 3-22) (the preprocessor is the interpreter).

13. As per claim 10:

The system according to claim 9, wherein the operand stack is a mixed stack comprising a register stack and a memory stack (column 11, lines 15-22).

14. As per claim 11:

The system according to claim 10, wherein the register stack comprises at least one register to hold at least one respective top element of the stack and the memory stack comprises a contiguous memory region to hold the remaining elements of the operand stack (column 3, lines 15-22).

15. As per claim 12:

A machine accessible medium containing program instructions that, when executed by a processor, cause the processor to perform a series of operations comprising:

translating a virtual machine instruction into threaded code based on an operand stack state of the virtual machine instruction (column 11, lines 3-22);

dispatching the virtual machine instruction according to the operand stack state (inherent); and

executing the instruction (inherent).

16. As per claim 13:

The machine accessible medium according to claim 12, wherein the threaded code is based on an entry point into shared execution code (column 11, lines 3-22) (it is an entry into a subroutine).

17. As per claim 14:

The machine accessible medium according to claim 12, further containing program instructions that, when executed by the processor cause the processor to perform further operations comprising:

determining a number of operands that are present on an operand stack at a time before the virtual machine instruction is executed (column 11, lines 3-22) (It is inherent that this step will be taken in moving items from registers to memory and adjusting the SP for the instructions);

determining a number of operands that are present on the operand stack at a time after the virtual machine instruction is executed (column 3, lines 3-22); and

inferring a number of shift operations required to maintain top-of-stack elements after the virtual machine instruction is executed (column 3, lines 3-22).

18. As per claim 15:

The machine accessible medium according to claim 13, wherein the wherein the number of shift operations required after execution of the instruction is based on the number of operands present on the operand stack at a time before the instruction is executed and the number of operands present on the operand stack at a time after the instruction is executed (column 11, lines 15-22).

19. As per claim 16:

The machine accessible medium according to claim 13, wherein the number of shift operations required after execution of the instruction is inferred based on a static lookup table (column 6, lines 39-47) (The translation is based on a static table. Through the table, it is known how many operands will be used and how many will be placed back on the stack, and based on that is how many items are transferred to memory.).

20. As per claim 17:

The machine accessible medium according to claim 12, wherein the operand stack state comprises a number of shift operations to maintain top-of-stack elements of an operand stack after execution of the virtual machine instruction (column 11, lines 15-22).

21. As per claim 18:

The machine accessible medium according to claim 17, wherein the top-of-stack elements comprise a register stack (column 11, lines 15-22).

22. As per claim 19:

The machine accessible medium according to claim 12, further containing program instructions that, when executed by the processor cause the processor to perform further operations comprising:

execute a number of shift operations to replace top-of-stack elements to an operand stack (column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

23. As per claim 20:

The machine accessible medium according to claim 19, wherein the number of shift operations is based on a number of elements on the operand stack that are consumed by the virtual machine instruction and a number of elements that are produced by the virtual machine instruction (column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

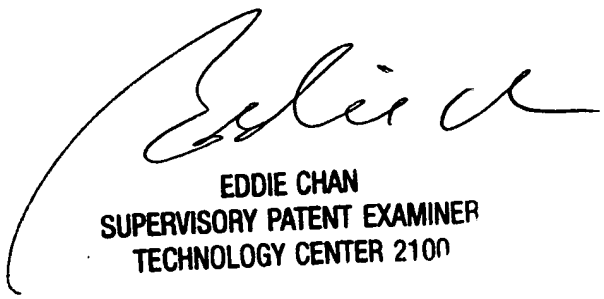
King et al. (US Patent 3200379) shows that mixed stacks and methods for moving stack items between registers and memory is extremely well known in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
Art Unit 2183



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